REMARKS

Reconsideration of the application is respectfully requested.

The undersigned would initially like to thank the Examiner for the telephone interview of May 9, 2006, in which the undersigned and Examiner Tabone discussed the subject matter of claims 1 and 16 in view of the relied upon art reference of U.S. Patent No. 6,370,661 issued to Miner ("Miner"). One of the points made during that interview, on behalf of the Applicants, is that the claimed MTE is not just integrated with, but also shares the same memory interface as its respective bus controller. This requires that the testing functions by the MTE, as well as non-testing functions or "data traffic" by the processor, be performed upon the associated memory using the same memory interface. Miner, however, discloses **separate** interfaces within the microprocessor, to access the memory 510. The external test controller 580 only uses the test management logic 570 ("interface") to access the memory, whereas normal peripheral circuits only use the bus unit 530 ("interface") to access the same memory 510.

Another point made by the Applicants during the interview is that the mere duplication of elements 560, 570, and 530 of Miner would also require duplicating their **respective** buses 554, 575. That is different than the limitations in Applicants' claim 16 in which the same bus is used to pass both normal data traffic and test traffic to memory, using each of a number of bus controllers for the same bus. The duplication of Miner's bus 554 and test bus 570 does not teach or suggest combining them into the same bus, as Applicants are not aware of the concept of a bus being "embedded" with another bus.

Based on the interview, the independent claims have been revised here to more clearly reflect the distinctions that have been argued, without introducing any new matter. For instance, in claim 1, the amended subject matter has been sourced from original claim 2, as well as paragraph [0010] of the Specification as filed.

As to claim 16, this claim has been amended to more clearly reflect the intention that the bus controllers are **for the same bus** that is used to transmit initiation signals from the processor to the respective memory testing engines. This is also the same bus that the processor uses to access the memories via the respective bus controllers for non-

testing data traffic. Miner does not teach or suggest such operations because in Miner, if multiple microprocessors were to be coupled to the test controller 580, each of these microprocessors, including their built-in test units, would have to be accessed over a separate bus. In addition, any "bus controller" of Miner that is used by the test controller to access the memories is different from another "bus controller" that is used by normal peripheral circuits that are connected to the microprocessor. Accordingly, claim 16 is not taught or suggested by Miner.

Turning now to claim 30, this claim has also been amended to clarify that there are instructions executable by a machine to perform a method in which each of a number of memories that is associated with a respective ASIC is accessed over the same bus, and where each memory is accessed via a respective utility bus slave (UBS) controller on the respective ASIC. Each UBS controller has its associated memory testing engine with which the controller shares a memory interface to the memory associated with the respective ASIC. Each MTE is configured by writing to a respective one of the UBS controllers, over the same bus. Such parallel channels over the same bus are not taught or suggested by Miner, because in Miner, each microprocessor (with its built-in test circuitry) is coupled to the test controller 580 by its separate, dedicated test bus 575. If multiple microprocessors were present in Miner, each would have its own separate test bus for testing the memory, and a separate normal bus 554 for normal (non-test) accesses to the same memory. This does not teach or suggest Applicants' capability in claim 30 for accessing multiple ASICs in parallel and configuring the memory testing engines in each ASIC, over the same bus.

Finally, claim 44 has also been amended to clarify multiple memory testing means that can operate at once, and that are to be accessed as part of respective bus controllers for the same bus that is used for non-test access to the memories. Expanding Miner to test multiple microprocessor memories (using the test controller) does not teach or suggest the means in Applicants' claim 44.

Any dependent claims not mentioned above are submitted as being neither anticipated nor obvious, for at least the same reasons given above in support of their base claims.

It should be noted that not all of the assertions made in the Office Action, particularly those with respect to the dependent claims, have been addressed here, in the interest of conciseness. Applicants reserve the right to challenge any of the assertions made in the Office Action by the Examiner, with respect to the relied upon art references and how they would relate to Applicants' claim language.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: May 18, 2006

By _____
Farzad E. Amini, Reg. No. 42,261

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on May 18, 2006.

_____
Margalux Rodriguez *May 18, 2006*